Analysis of Common Power Factor Correction Topologies in Switch-Mode Power Supplies

Rafał Kasikowski
Lodz University of Technology, Faculty of Electrical, Electronic, Computer and Control Engineering, Institute of Electronics, al. Politechniki 8, 93-590 Łódź

Abstract: Nonlinear load characteristics intrinsic to switch-mode power converters lead to elevated harmonic distortion levels in the AC mains. This power quality degradation must be counteracted by implementing Power Factor Correction (PFC) techniques, frequently in the form of supplementary modular circuitry. The most widely adopted solution employs an active PFC configuration comprising inductive components and power switches that regulate and modify the converter's input current, shaping it to mirror both the phase and waveform of the input voltage. This modelling of the mains current shape can be performed by means of various PFC topologies combined with distinct conduction modes of the PFC inductor. This paper provides an overview of PFC circuitry designs, including boost-type topologies and their derivatives, the flyback-topology-based configuration, and the bridgeless totem-pole architecture noted for its superior power conversion efficiency. A detailed theoretical analysis of the power factor correction problem is presented, along with descriptions of the main operational characteristics of the examined PFC topologies. The study is further supported by oscilloscope screenshots captured from real, physical PFC modules, either designed by the author (boost and flyback-based topologies) or acquired for the purposes of this research.

Keywords: power electronics, AC/DC converters, power factor correction, bridgeless totem-pole, power losses

1. Introduction

Defined as the ratio of active power to apparent power, power factor quantifies how effectively energy is transmitted between the input power source and the output of a given device, in this instance, a switch-mode power supply (SMPS). Active power, quantified in Watts, corresponds to the power dissipated by the load, whereas apparent power refers to the total power transfer, comprising both active and reactive elements, between the source and load [1, 2]. A unity power factor denotes an ideal scenario where all apparent power is delivered as active power with no reactive power present. Under these conditions, the voltage and current waveforms exhibit identical shapes, share the same harmonic content, and remain in phase with each other. The foregoing is satisfied in the case of linear resistive loads, where the power factor attains its maximum value of unity. In electrical systems where the input voltage is free of harmonics but the load exhibits nonlinear behaviour, or in cases where both voltage and current waveforms contain higher-order harmonics that are not mutually correlated, the active power diverges from the apparent power. As a result, the power factor falls below unity. The introduction of harmonics causes an increase in the root-mean-square (RMS) values of the waveforms, which frequently does not correspond to an increase in active power transfer. Of particular concern are raised RMS current levels that do not improve active power but contribute to system losses, calculable by the following relation, Eq. 1:

$$P_{loss} = I_{RMS}^2 \cdot R \tag{1}$$

where R represents resistances in a given system, Ω.

Power transfer resulting in elevated losses and without contribution to energy delivery at the load is undesirable, and thus the primary concern is the transmission of active power alone.

In general terms, the instantaneous power $p(t)$ (refer to Fig. 1) transmitted through electrical networks is the product of the instantaneous current $i(t)$ and the instantaneous voltage $v(t)$, Eq. 2 [14]:

$$p(t) = i(t) \cdot v(t) \tag{2}$$

The average instantaneous power, or in other words active power P, is derived by integrating the instantaneous power over a specific period T. Eq. (3):

$$P = \frac{1}{T}\int_0^T p(t) \cdot dt = \frac{1}{T}\int_0^T i(t) \cdot v(t) \cdot dt \tag{3}$$

Autor korespondujący:
Rafał Kasikowski, rafal.kasikowski@p.lodz.pl

Artykuł recenzowany
nadesłany 06.10.2025 r., przyjęty do druku 12.01.2026 r.

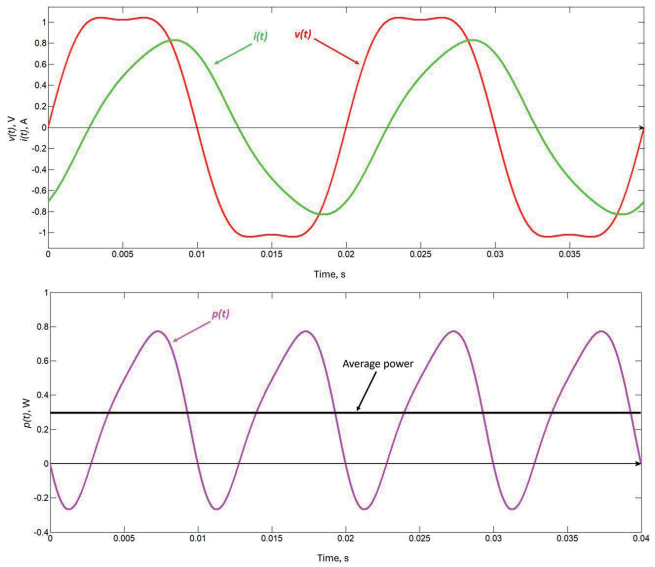

Fig. 1. Instantaneous voltage and current (top), instantaneous power and average (active) power (bottom)
Rys. 1. Przebiegi chwilowego napięcia i prądu (u góry) oraz mocy chwilowej i średniej wartości (czynnej) mocy (na dole)

The instantaneous current waveform $i(t)$ and voltage waveform $v(t)$, illustrated in Fig. 1 are time-shifted and exhibit harmonic distortion, indicative of non-sinusoidal behaviour with multiple frequency components. Periodic signals of this nature are generally representable in the amplitude-phase form of a Fourier series [3], where the index n corresponds to the harmonic component number, Eq. 4:

$$v(t) = V_0 + \sum_{n=1}^{\infty} V_n \cdot \cos(n\omega t)$$

$$i(t) = I_0 + \sum_{n=1}^{\infty} I_n \cdot \cos(n\omega t - \varphi_n) \tag{4}$$

$$P = \frac{1}{T}\int_0^T i(t) \cdot v(t) \cdot dt = V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cdot \cos(\varphi_n)$$

where: V_0 – average value or DC component of the voltage waveform, V; I_0 – average value or DC component of the current waveform, A; V_0, I_n – amplitudes of the n^{th} voltage and current harmonics, V, A; $\omega = \frac{2\pi}{T}$, rad/s; φ_n – the phase shift between voltage and current waveform at n^{th} harmonic, rad.

Analysis of the average (active) power equation reveals that active power is only delivered to the load for harmonic components whose frequencies are present in both the voltage and current waveforms. Harmonics present in the current but absent in the voltage, or vice versa, do not contribute to the transmission of active power. Moreover, the phase shift angle φ_n between corresponding harmonic components of voltage and current impacts the magnitude of active power, attaining its maximum value when these components are in phase, i.e., when $\varphi_n = 0$ and $\cos(\varphi_n) = 1$.

In nonlinear electrical circuits, such as rectifiers and SMPSs, the AC line voltage generally maintains a nearly pure sinusoidal waveform, typically comprising only the fundamental frequency. Conversely, the current waveform can exhibit a range of harmonic frequencies with varying phase angles. Under these conditions, the active power is exclusively governed by the fundamental harmonic, as only this harmonic contributes to the actual transfer of active power, Eq. 5.

$$P = \frac{V_1 I_1}{2} \cdot \cos(\varphi_1) \tag{5}$$

The other harmonic components of the current waveform, however, increase RMS value of the current, Eq. 6:

$$I_{lRMS} = \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}} \tag{6}$$

As indicated previously, the power factor (PF) defines how effectively electrical energy is transmitted. Specifically, it is the ratio of active power to apparent power, with the latter being the product of the RMS values of current and voltage, Eq. 7.

$$PF = \frac{P}{V_{RMS} \cdot I_{RMS}} \tag{7}$$

Replacing Eq. 7 with the previously established expressions, we find, Eq. 8:

$$PF = \frac{\frac{V_1 I_1}{2} \cdot \cos(\varphi_1)}{\frac{V_1}{\sqrt{2}} \cdot \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} = \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \cdot \cos(\varphi_1) \tag{8}$$

where $\frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}}$ is referred to as the distortion factor.

As noted above, the distortion factor is defined as the ratio between the RMS value of the current's fundamental component and the RMS value of the total current, whereas $\cos(\varphi_n)$ represents the phase displacement factor. Thus, when the AC voltage waveform is a pure sine wave, the power factor equals the product of these two quantities. The power factor ranges from 0 to 1.

Literature often employs the term THD (Total Harmonic Distortion) [4] to describe the extent of harmonic content present. Commonly, this measurement is defined as the ratio of the RMS values of the higher harmonic frequencies (excluding the fundamental and assuming no DC offset) to the RMS value of the fundamental frequency, Eq. 9:

$$THD = \frac{\sqrt{\sum_{n=1}^{\infty} \frac{I_n^2}{2}}}{\frac{I_1}{\sqrt{2}}} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{9}$$

Power converters, due to their nonlinear load characteristics, induce a high level of mains harmonics, thereby necessitating the implementation of power factor correction to maintain effective energy transmission. Typically, the input section of an SMPS comprises a rectification stage followed by an energy storage capacitor. This capacitor is generally large enough to hold a voltage close to the peak magnitude of the input sinusoidal voltage waveform, requiring recharging only at successive peaks. The process involves rapidly charging the capacitor with a large current pulse, then allowing it to discharge gradually into the load until the next cycle begins (Fig. 2). The PFC stage is usually implemented by active circuits involving power

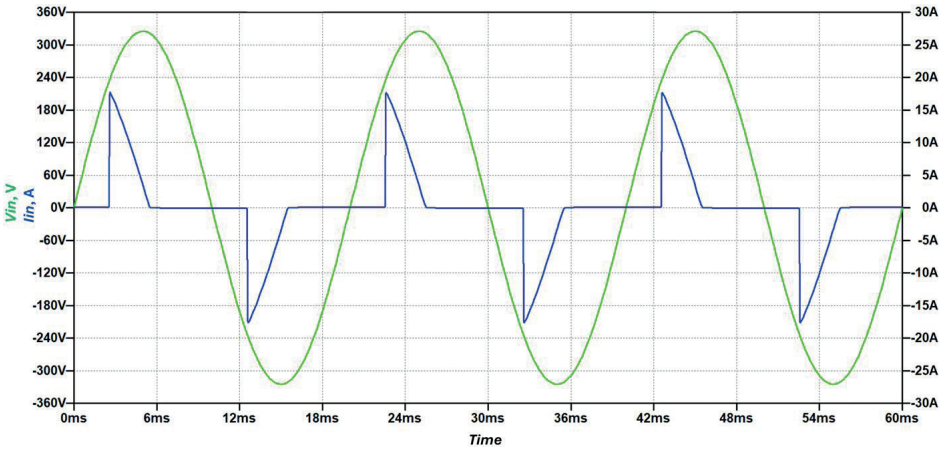

Fig. 2. Input characteristics of typical SMPS without PFC. Input voltage (green), input current (blue)
Rys. 2. Charakterystyka wejściowa typowego zasilacza impulsowego bez korekcji współczynnika mocy; napięcie wejściowe (zielony), prąd wejściowy (niebieski)

transistors, integrated circuits (ICs), and magnetic components to comply with international regulations on current harmonics, which generally require power supplies of certain classifications and with power consumption above specified limits to be equipped with PFC controllers [15]. This paper presents an overview of active PFC circuit designs covering the boost-based topology and its variants, the flyback-topology configuration, and the bridgeless totem-pole architecture. It also details their practical implementation and evaluates key performance parameters, namely power factor, efficiency of power conversion, and total harmonic distortion.

2. Boost-type PFC topology

Active PFC modules adjust the current entering the converter so that its waveform and phase closely align with the input voltage. This precise shaping of the input current waveforms ensures a high power factor, maximizing the active power drawn from the power grid while significantly reducing THD and input current harmonics. Active PFC circuits can be implemented using various design topologies, with the step-up (boost--type) converter being a popular choice [5].

The main boost-type PFC topologies include conventional boost PFC (Fig. 3), which uses a diode bridge rectifier followed by a boost converter stage. Another form is the interleaved boost PFC, where two or more boost converters operate in parallel, often with phase shifts to reduce input current ripple, improve efficiency, and decrease output voltage ripple, all of which are particularly advantageous in higher-power or efficiency-sensitive applications [16]. The bridgeless boost PFC further enhances efficiency by eliminating the diode bridge, and hence substantially reducing conduction losses.

In conventional boost PFC converters, operation modes generally include discontinuous conduction mode (DCM), continuous conduction mode (CCM), and critical conduction mode (CrCM), with CrCM often paired with quasi-resonant (QR) control of the power switch, a technique also known as valley switching. Integration of all conduction modes into a singular IC is frequently observed to enable improved control over the performance parameters of the PFC module [17, 18]. The PFC inductor current waveforms for individual modes of operation are illustrated in Fig. 4. The waveforms sketched in Fig. 4 are simplified and show only a few switch-on and switch-off cycles of the PFC power switch, whereas the oscilloscope screenshots capture a very narrow time interval near the peak of the input sinusoidal voltage. The captured PFC inductor current is shown in blue, and the drain-to-source voltage of the power switch is shown in red. The design of the PFC choke, the operating frequency, and the chosen conduction mode determine how many individual on-off cycles of the switch occur within a single half-cycle of the AC input voltage.

As can be inferred from the simplified representation of the PFC inductor current waveforms, the magnitude of the maximum inductor current changes in accordance with the sinusoidal input voltage. By analysing the PFC coil current waveform in terms of the mains frequency (50 Hz), the current measured at the converter's input terminals, I_{AC}, corresponds to the averaged inductor current, I_{AVER}, meaning it is sinusoidal and free from switching frequency components (Eq. 10).

$$I_{AVER} = I_{AC} \tag{10}$$

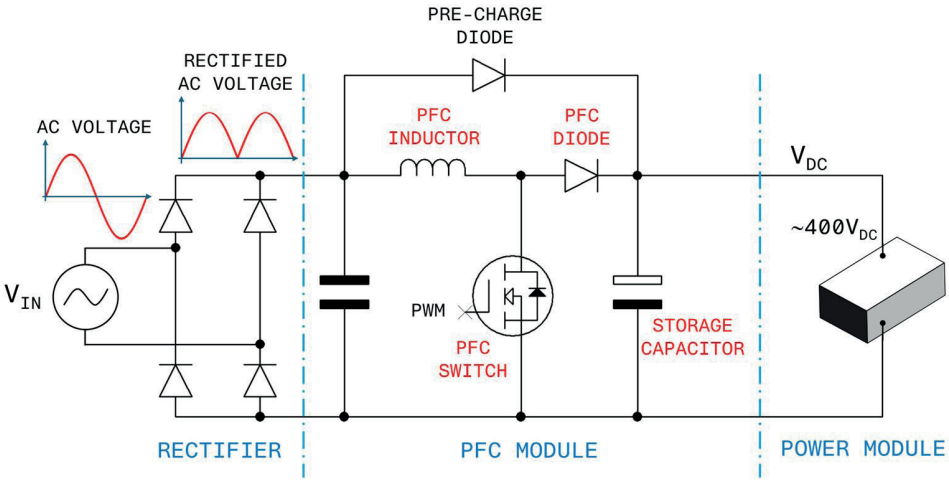

Fig. 3. Conventional PFC boost topology
Rys. 3. Typowa architektura przetwornicy PFC typu boost

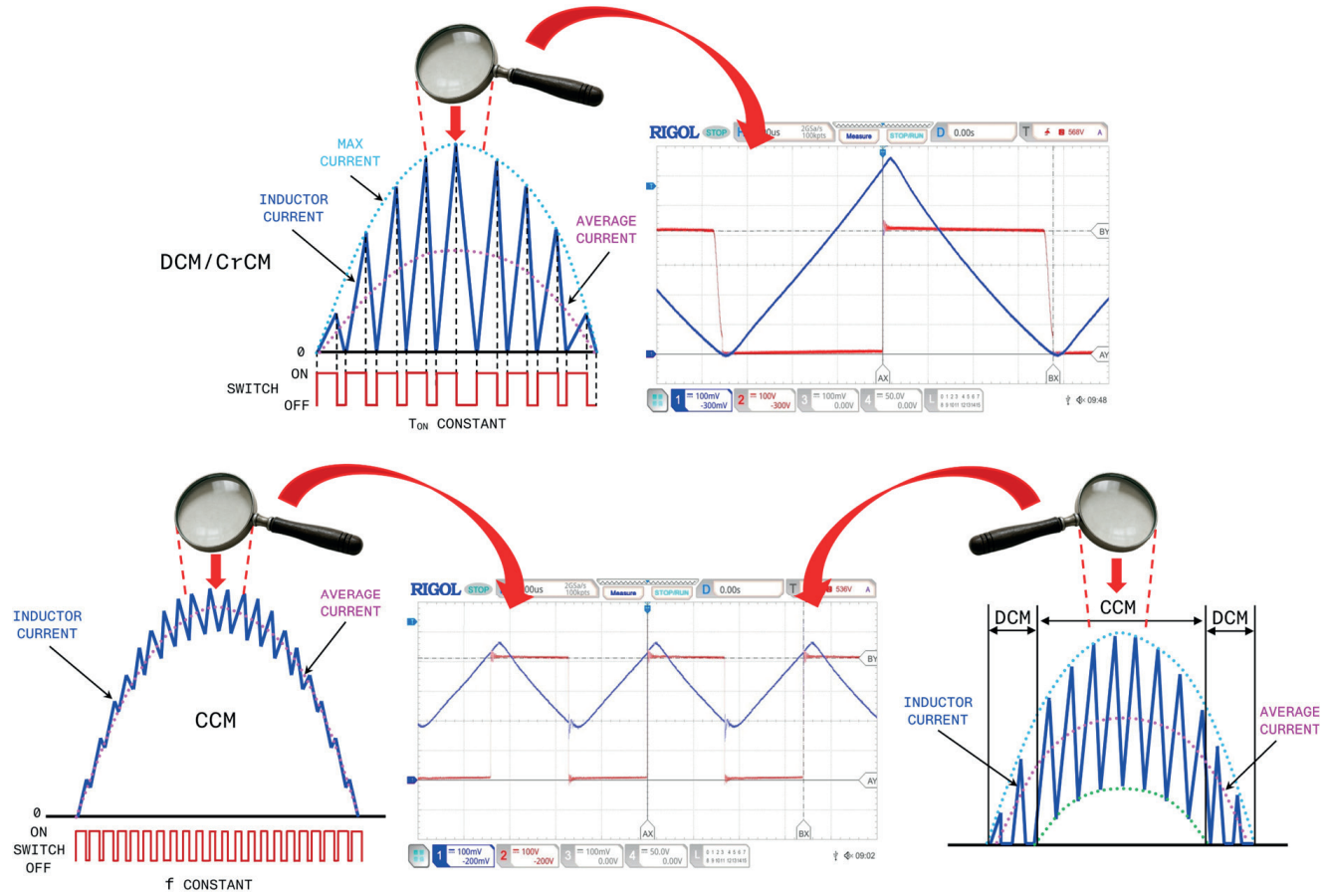

Fig. 4. PFC inductor currents for various operating modes. CrCM (top), CCM (bottom left), mixed-mode operation (bottom right)
Rys. 4. Przebiegi prądu cewki PFC dla różnych trybów pracy. CrCM (na górze), CCM (na dole z lewej), tryb mieszany (na dole z prawej)

One significant aspect of the PFC module operating in CrCM is that the conduction time of the power switch, T_{ON}, remains constant, while the OFF periods vary, causing the switching frequency to change over time. The following can be deduced from the corresponding waveform (Eqs. 11–16):

$$I_{AVER} = \frac{I_{MAX}}{2} \tag{11}$$

When the transistor is in the ON state, the voltage across the inductor is essentially equal to V_{AC} (the peak sinusoidal voltage at a given time), and the current flowing through the inductor tends to increase proportionally to the ratio of the voltage across the inductor to the inductance L:

$$I_{MAX} = \frac{V_{AC} \cdot T_{ON}}{L} \tag{12}$$

Assuming that PF is close to unity, at the converter's input we observe:

$$P_{IN} = V_{RMS} \cdot I_{RMS} \tag{13}$$

By using the equivalence of the averaged PFC coil current I_{AVER} and the input current to the converter I_{AC}, the above equation can be written as:

$$P_{IN} = V_{RMS} \cdot I_{AVER_{RMS}} = \frac{V_{RMS} \cdot I_{AVER}}{\sqrt{2}} = \frac{V_{RMS} \cdot I_{MAX}}{2\sqrt{2}} \tag{14}$$

By comparing the maximum current values through the PFC coil I_{MAX} as indicated in Eq. 12 and Eq. 14, we derive:

$$\frac{2\sqrt{2} \cdot P_{IN}}{V_{RMS}} = \frac{V_{AC} \cdot T_{ON}}{L} \tag{15}$$

Hence, ultimately:

$$T_{ON} = \frac{2 \cdot P_{IN} \cdot L}{V_{RMS}^2} \tag{16}$$

To conclude, the conduction time of the power switch, T_{ON}, in CrCM remains fixed for a given RMS value of the input voltage and power drawn from the input source.

In PFC modules operating in CCM, the switching frequency is typically maintained at a constant value, while multi-mode operation enables the use of various modes to maximize the efficiency of power conversion across different loads, using DCM for light loads and CCM for heavier loads.

3. Flyback-based PFC

PFC modules based on the flyback topology are another popular choice among power electronics engineers due to the various advantages associated with this topology, although they are primarily used in relatively low-power applications. Not only does this configuration achieve a relatively high power factor, but it also provides isolation between input and output, a low component count, and a comparatively simple design and structure [6, 7]. In a typical flyback PFC converter configuration (Fig. 5), a diode bridge is followed by a capacitor filter and connected in series with the primary winding of the flyback transformer and its primary switch,

while the secondary winding is connected to a freewheeling diode and a relatively large output capacitor. The transformer's primary coil fulfils the role of the PFC inductor. Depending on the operating mode, the freewheeling diode on the secondary side either carries current continuously when the primary switch is off during a single switching period (CCM), or allows a current-free interval on the secondary side during this period (DCM). Similar to the boost converter topology, CrCM operation occurs when the diode current drops to zero exactly as the primary switch transitions to the ON state.

As shown in Fig. 5, the flyback-derived configuration can provide power factor correction, handle output voltage regulation, and offer input-to-output isolation – all within a single stage. This circuit operates similarly to a conventional boost PFC converter, but its output is taken from an isolated secondary winding on the boost PFC inductor rather than from a high-voltage diode placed directly after the inductor, as is typical in standard high-voltage boost modules. The input to the flyback PFC transformer, after the AC bridge rectifier, is a full-wave rectified sine wave at twice the line frequency (usually 100 Hz), rather than a regulated DC voltage (typically 400 V). This characteristic can be a disadvantage because the 100 Hz frequency component passes through the transformer and contributes to output voltage ripple. To minimize the impact of the capacitive input filter on power factor, the storage capacitor following the bridge rectifier must be kept small. Without a large input capacitor, the converter doesn't have much built-in hold-up time, other than what comes from the energy stored in the transformer and output capacitors.

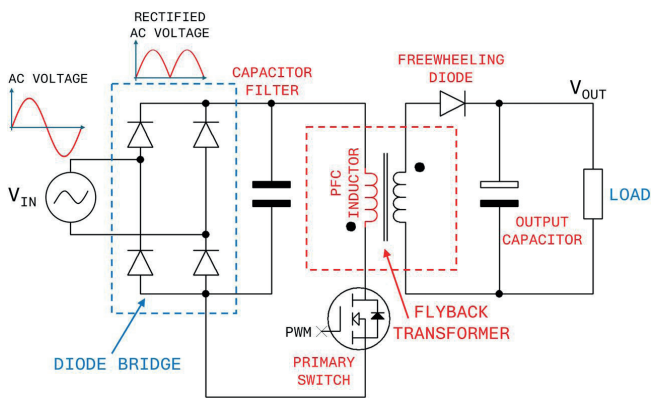

Fig. 5. Conventional flyback PFC converter
Rys. 5. Typowa architektura przetwornicy PFC typu flyback

Flyback PFC converters operating in CrCM typically employ constant ON-time control, which simplifies the control circuitry and contributes to their widespread use [8, 9]. The current waveforms of the transformer's primary winding and the drain-to-source voltage across the main switch for a PFC flyback-based converter, designed using an L6562 critical-conduction-mode PFC controller [19], are shown in Fig. 6. To achieve a better *PF*, the ON-time of the power switch is artificially lengthened by the circuit around the AC input voltage zero-crossings. This increase diminishes progressively with rising instantaneous AC voltage to become negligible as the line voltage increases towards the peak of the sinusoid.

As can be observed in Fig. 6, the CrCM mode operates similarly to a traditional boost PFC converter in critical conduction mode, where the switching frequency naturally varies as a function of the AC line input voltage and load conditions. Recovery losses in the output rectifier are negligible because the current in the secondary winding of the flyback transformer falls to zero before the main power switch is turned on again. This characteristic lends itself well to the use of transistor-based synchronous rectifiers in low-voltage, high-current designs, thereby reducing conduction losses in the output stage.

As with any flyback topology, the transformer's design and construction must follow an appropriate methodology to guarantee reliable operation of the PFC stage. This process also involves minimizing leakage inductance, reducing power loss, and maintaining electromagnetic emissions within regulatory standards.

The significant drawback of flyback-type PFC converters is their comparatively low efficiency of power conversion, a characteristic shared by all flyback-based converters, generally about 90 %. This stems from the unique structure of the flyback transformer, which, in fact, functions as two magnetically linked inductors. The energy storage phase inherent to this topology leads to high peak currents and requires magnetic cores with larger spatial dimensions and wider air gaps to prevent saturation and preserve the core's magnetic properties. These constraints limit its applications to relatively low power levels, where the efficiency penalty is acceptable for the benefits of the simplicity of the design, low component count, and hence, cost-effectiveness.

4. Bridgeless totem-pole PFC

The totem-pole topology is emerging as a promising alternative to traditional configurations and designs of PFC modules due to its enhanced power conversion efficiency and consistently high power factor [10–13]. However, the absence of dedicated control integrated circuits has thus far limited its widespread adoption. This topology is expected to see broad implementation in high-power, high-efficiency applications due to its ability to combine the advantages of traditional PFC approaches with the elimination of the conventional diode bridge rectifier. The traditional diode bridge is replaced with MOSFETs or SiC devices, and the architecture naturally facilitates the use of high-performance gallium nitride (GaN) transistors in the boost stage of the converter.

The totem-pole PFC (TPFC) topology extends the boost converter concept into the AC domain, incorporating modifications that enable bidirectional current flow and power factor correction, making it a functional and structural derivative of the boost converter. Figure 7 illustrates, in stages, the transition from the conventional boost PFC module into a TPFC architecture.

As shown in Fig. 7(d), the converter topology features two half-bridge sections: a high-frequency (fast) stage and an AC line frequency (slow) stage. The fast-switching devices operate at the relatively high PWM (Pulse-Width Modulation) frequency, performing the combined roles of both the switching element and diode in a traditional boost PFC, thereby enabling input current shaping and output voltage regulation. In contrast, the slow-switching section, operating at the AC line frequency, functions as a replacement for the conventional diode rectifier bridge. Due to their enhanced high-frequency characteristics, bidirectional current conduction capability, and elimination of reverse recovery concerns, GaN transistors are generally implemented as fast switching devices, while MOSFETs are predominantly applied as line-frequency switches. Figure 8 provides an illustration of the way TPFC operates during the positive and negative half-cycles of the line voltage. In the positive half line cycle, fast switch 1 is turned on to channel current through the inductor and subsequently deactivated to divert the current through fast switch 2, thereby transferring energy to the capacitor and load. Throughout this positive interval, the current flows back to the source via slow switch 1. During the negative phase, fast switch 2 is activated

Fig. 6. Primary winding current (green) and drain-to-source voltage across power switch (blue) along half-cycle of AC input voltage for flyback-based PFC converter built using L6562 controller

Rys. 6. Prąd uzwojenia pierwotnego (zielony) oraz napięcia dren-źródło tranzystora mocy (czerwony) dla półokresu napięcia wejściowego w przetwornicy PFC typu flyback zbudowanej na bazie kontrolera L6562

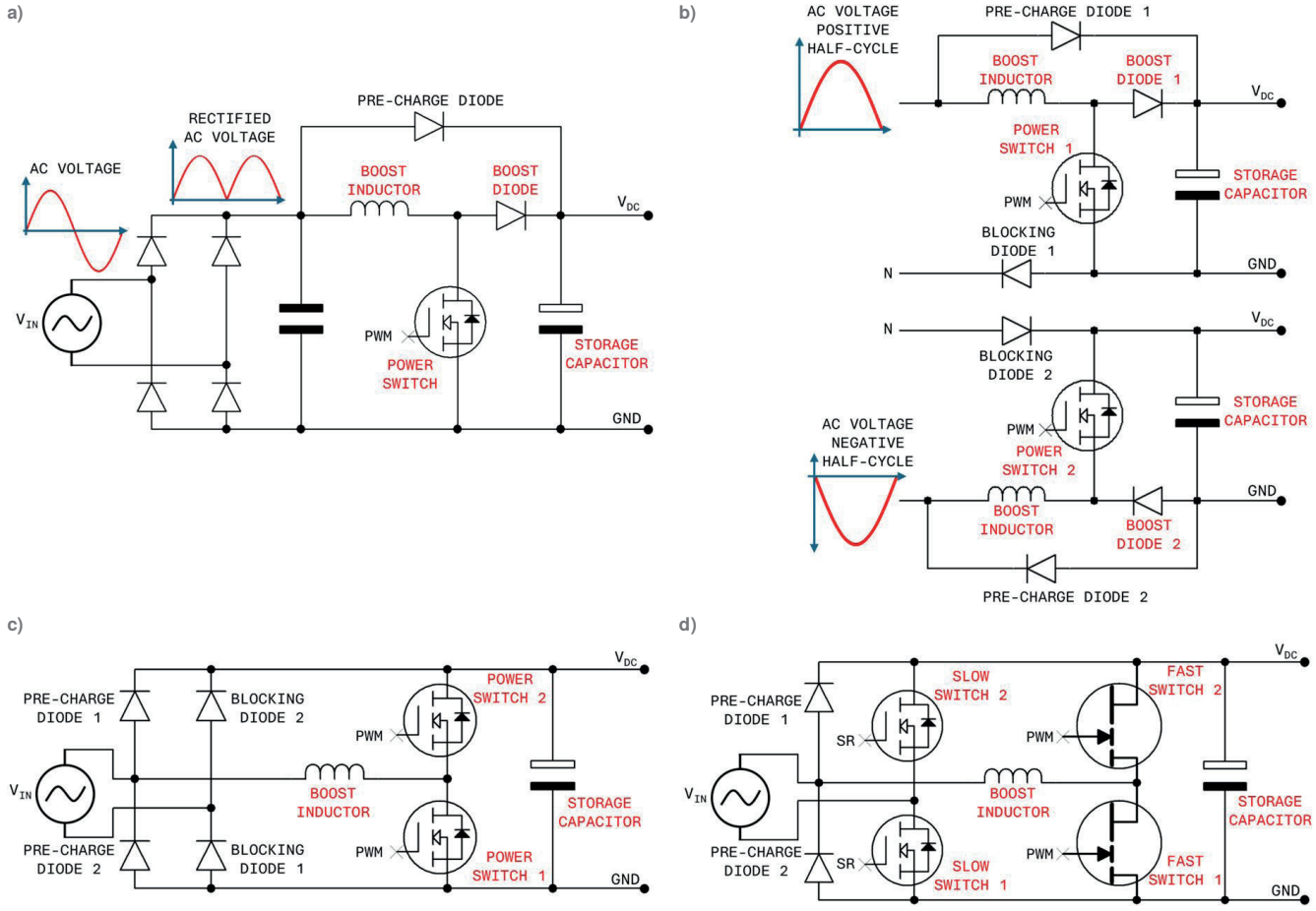

Fig. 7. Derivation of totem-pole topology: a) conventional boost PFC, b) positive and negative half-cycle boost PFC, c) totem-pole PFC using diodes, d) totem-pole PFC using synchronous rectification and fast GaN transistors

Rys. 7. Wyprowadzenie topologii totem-pole: a) Typowy PFC typu boost, b) PFC typu boost dla dodatniej i ujemnej połówki napięcia wejściowego, c) totem-pole PFC z użyciem diod, d) totem-pole PFC z prostowaniem synchronicznym i szybkimi tranzystorami typu GaN

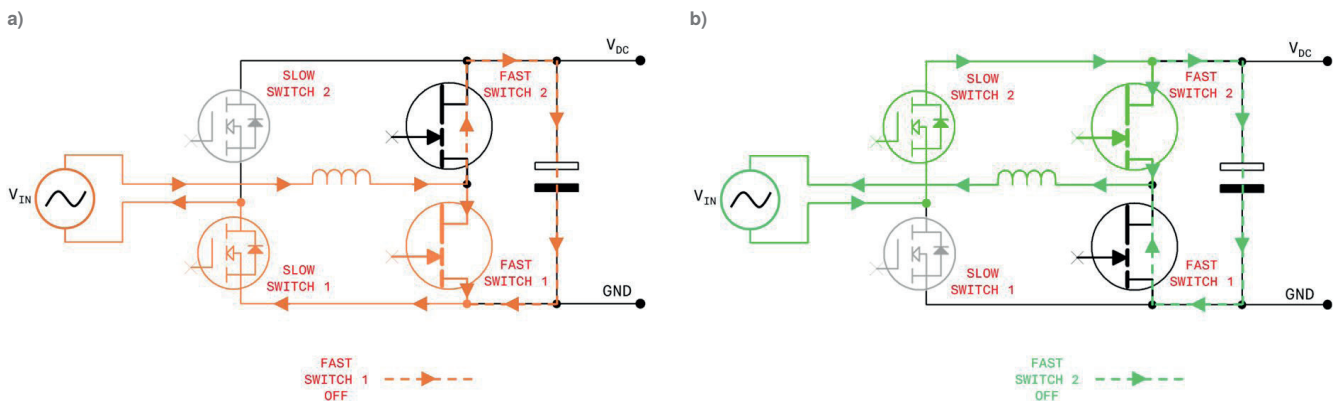

Fig. 8. Equivalent TPFC circuit during positive half-line cycle (left), and negative half-line cycle (right)

Rys. 8. Równoważny obwód TPFC podczas dodatniej połówki napięcia wejściowego (z lewej) oraz ujemnej połówki napięcia wejściowego (z prawej)

Table 1. Performance parameters for investigated PFC topologies

Tabela 1. Parametry pracy badanych topologii PFC

AC Voltage		100 V RMS			230 V RMS		
Parameter		PF	THD	Efficiency	PF	THD	Efficiency
PFC Topology	Flyback (CrCM) 40 W	0.987	12.38 %	89.73 %	0.942	16.71 %	91.66 %
	Boost (Multi-Mode) 300 W	0.996	4.24 %	90.4 %	0.913	25.78 %	96.1 %
	Totem-Pole PFC (Multi-Mode) 400 W	0.998	3.67 %	96.01 %	0.994	4.2 %	98.3 %

to guide current through the inductor opposite to the direction observed during the positive phase, then turned off to reroute the current through fast switch 1, enabling energy delivery to the capacitor and load. The current returns to the source via slow switch 2 over the course of the negative interval.

Similar to other PFC topologies, the TPFC architecture is capable of operating in DCM, CrCM, CCM, or under a multimode control regime [20, 21]. Seamless transitions between these operational modes, correlated with variations in output power levels, enable an enhanced efficiency of power conversion across a wide operating range.

5. Performance parameters of PFC topologies

Three PFC modules (Fig. 9), each corresponding to one of the investigated topologies, were subjected to evaluation of their key performance parameters, specifically power factor, efficiency of power conversion, and THD. The tests were conducted sequentially at two distinct input voltage conditions. The devices were initially connected to an AC power source set to 100 V RMS. After completing the first set of measurements, the input voltage was increased to 230 V RMS to analyse performance under the standard input voltage range found in most countries. Prior to the measurements, the PFC converters were continuously operated at the power level corresponding to their power handling capability until they reached thermally steady-state conditions. The measured performance parameters were put together for comparison in Tab. 1.

The 40 W flyback PFC converter, shown in Fig. 9, was designed by the author using an L6562 critical-conduction-mode PFC controller [19]. As can be read from Tab. 1, its PFC circuit is capable of achieving a very high power factor at both the low input voltage and the high input voltage. Specifically, at lower input voltages, as its true for all PFC topologies, the values of power factor approach almost unity. This is due to the higher PFC inductor currents required to deliver the same power level at lower input voltages, which allows for better control of the current waveform and its shaping across the entire AC cycle, resulting in improved alignment with the input voltage waveform. The drawback of this PFC solution, as expected, is its relatively low efficiency of power conversion compared to the other PFC converters.

The boost-type PFC module evaluated in this study was also developed by the author, employing an NXP TEA2017AAT digital configurable multimode boost-type PFC controller [17]. The module was designed and tested to operate at a nominal output power of 300 W. As indicated in Table 1, the power factor correction and efficiency parameters achieved exceptionally high values, exceeding 90 % of the theoretical optimum for both evaluation criteria.

The bridgeless totem-pole PFC converter shown in Fig. 9 was purchased for the purposes of this research [22]. In this case the performance parameters of the TPFC module were investigated for the output power of 400 W. The totem-pole topology proved to be capable of achieving a superior efficiency of power conversion combined with a very high power factor.

6. Conclusion

This research focused on three commonly implemented topologies in power factor correction modules: a boost-based PFC circuit, a flyback-type PFC circuit, and a high-performance, high-power bridgeless totem-pole PFC circuit. The paper includes a detailed theoretical examination of the power factor correction issue, as well as an overview of the primary operational parameters of the investigated PFC topologies. Further support for the study is provided by oscilloscope images captured from actual physical PFC modules.

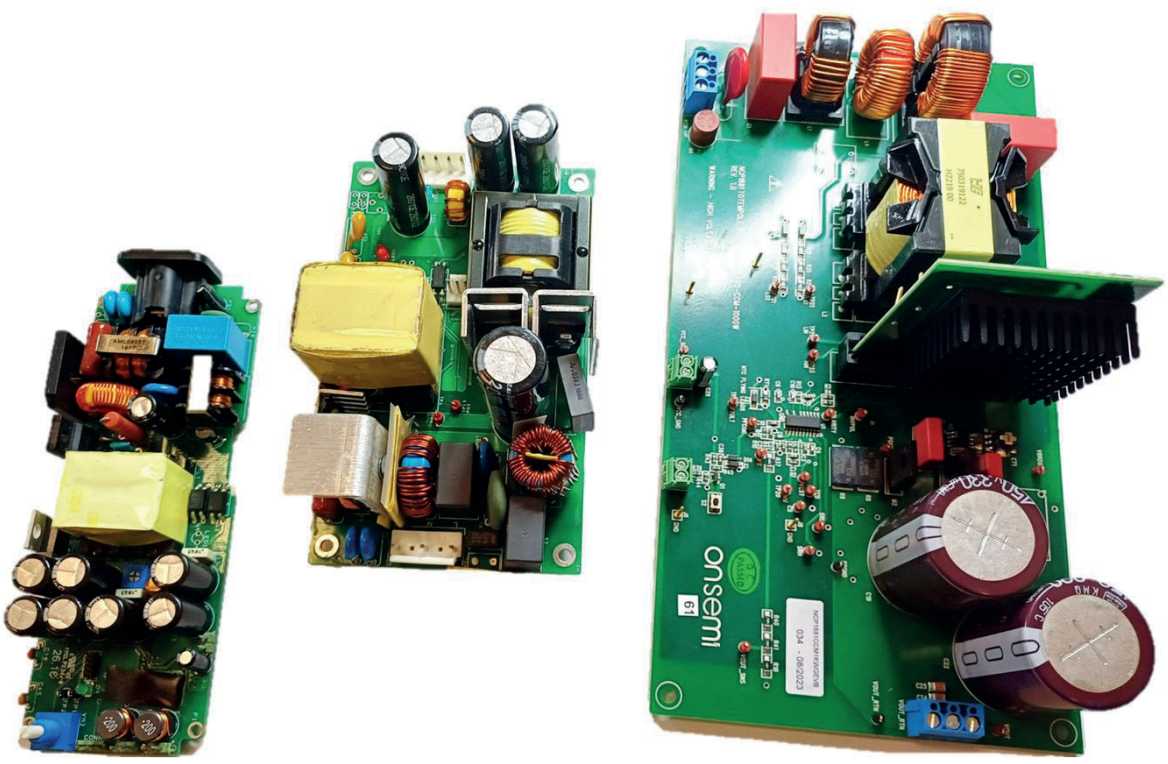

Fig. 9. Investigated PFC modules. Flyback-type CrCM PFC (left), boost-type multi-mode PFC (middle) and bridgeless totem-pole PFC (right)
Rys. 9. Badane moduły PFC. PFC typu flyback CrCM (z lewej), PFC typu boost w trybie mieszanym (środek) oraz bezmostkowa topologia totem-pole PFC (z prawej)

The discussed and evaluated boost-type PFC module operating in a multi-mode and the flyback-based PFC converter operating in DCM/CrCM were designed and constructed by the author of this article. The PFC module developed based on the bridgeless totem-pole topology was sourced externally for experimental analysis in this research. All PFC circuits were evaluated for their key performance parameters, namely power factor, efficiency of power conversion, and total harmonic distortion.

As shown in Table 1, all tested topologies are capable of achieving a very high power factor at both the low input voltage and the high input voltage. The flyback converter demonstrated a power factor close to unity, particularly at lower input voltages, which is attributed to enhanced control of the inductor current waveform at these voltages. However, the flyback-based topology exhibited the lowest efficiency of power conversion among the tested topologies. The boost topology delivered a balanced performance, achieving power factor and efficiency values exceeding 90 % at both voltage levels.

The totem-pole PFC topology achieves superior efficiency combined with a very high power factor. These findings suggest that while relatively simpler topologies like flyback and boost provide adequate performance for lower-to-medium power levels, the totem-pole configuration is more advantageous for high-power applications requiring stringent power quality and efficiency criteria.

Acknowledgments

This research is part of a project funded by the National Centre for Research and Development under the LIDER XV program, based on the contract for the execution and financing of the project No. LIDER15/0205/2024.

References

1. Fryze S., *Moc czynna, bierna i pozorna w obwodach o przebiegach odkształconych prądu i napięcia*, „Przegląd Elektrotechniczny", Vol. 7, 1931, 193–203.
2. Czarnecki L.S., *Currents' Physical Components (CPC) concept: A fundamental of power theory*, International School on Nonsinusoidal Currents and Compensation, Lagow, Poland, 2008, DOI: 10.1109/ISNCC.2008.4627483.
3. Erickson R.W., Maksimovic D., *Fundamentals of Power Electronics*, Springer International Publishing, 2020, DOI: 10.1007/978-3-030-43881-4.
4. Nunez-Ramirez V., Guerrero-Rodriguez NF., Batista-Jorge RO., Mercado-Ravelo R., Ramirez-Rivera F.A., Ferreira JA., Ramos-Ciprian RD., *Harmonic distortion caused by non-linear household loads: Measurement and modelling*, "Results in Engineering", Vol. 25, 2025, DOI: 10.1016/j.rineng.2025.104483.
5. Figueiredo J.P.M., Tofoli F.L., Silva B.L.A., *A Review of Single-Phase PFC Topologies Based on The Boost Converter*, 9th IEEE/IAS International Conference on Industry Applications – INDUSCON 2010, Sao Paulo, Brazil, 2010, DOI: 10.1109/INDUSCON.2010.5740015.
6. Luo H., Zang TL., Chen S., Zhou BX., *An Adaptive Off--Time Controlled DCM Flyback PFC Converter With Unity Power Factor and High Efficiency*, "IEEE Access", Vol. 9, 2021, 22493–22502, DOI: 10.1109/ACCESS.2021.3055248.
7. Lamar DG., Arias M., Rodriguez A., Fernandez A., Hernando MM., Sebastian J., *Design-Oriented Analysis and Performance Evaluation of a Low-Cost High-Brightness LED Driver Based on Flyback Power Factor Corrector*, "IEEE Transactions on Industrial Electronics", Vol. 60, No. 7, 2013, 2614–2626, DOI: 10.1109/TIE.2012.2196905.
8. Yan TS., Xu JP., Zhang F., Sha J., Dong Z., *Variable--On-Time-Controlled Critical-Conduction-Mode Flyback PFC Converter*, "IEEE Transactions on Industrial Electronics", Vol. 61, No. 11, 2014, 6091–6099, DOI: 10.1109/TIE.2014.2311401.
9. Kavci M., Tekin A., Tarhan C., *Total Harmonic Distortion and Power Factor Improvement Technique for CRM Flyback PFC Converters*, IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), Dallas, Texas, USA, 2019, DOI: 10.1109/MWSCAS.2019.8885187.
10. Huang QY., Huang Alex Q., *Review of GaN totem-pole bridgeless PFC*, "CPSS Transactions on Power Electronics and Applications", Vol. 2, No. 3, 2017, 187–196, DOI: 10.24295/CPSSTPEA.2017.00018.
11. Liu ZY., Lee FC., Li Q., Yang YC., *Design of GaN-Based MHz Totem-Pole PFC Rectifier*, "IEEE Journal of Emerging and Selected Topics in Power Electronics", Vol. 4, No. 3, 2016, 799–807, DOI: 10.1109/JESTPE.2016.2571299.
12. Meng FG., Shu Y., Wu JM., Yong SR., Chen YF., *A Mixed Conduction Mode Control Strategy Based on Fixed Turn--off Time for Totem-Pole PFC Converter*, "IEEE Transactions on Power Electronics", Vol. 40, No. 10, 2025, 15768–15779, DOI: 0.1109/TPEL.2025.3578152.
13. Cho J., Kim S., Kim Y., Yea J., Han B., *Bridgeless Totem--Pole Resonant Single-Power-Conversion PFC Converter*, "IEEE Transactions on Power Electronics", Vol. 39, No. 11, 2024, 15257–15268, DOI: 10.1109/TPEL.2024.3436522.

Other sources

14. IEEE, Standard 1459-2010, IEEE Standard Definitions for the Measurement of Electric Power Quantities Under Sinusoidal, Nonsinusoidal, Balanced, or Unbalanced Conditions, IEEE Power and Energy Society, 2010, DOI: 10.1109/IEEESTD.2010.5439063.
15. IEC 61000-3-2 Electromagnetic compatibility (EMC) – Part 3-2: Limits – Limits for harmonic current emissions (equipment input current ≤ 16 A per phase).
16. ON Semiconductor, *NCP1632A 2-Phase Power Factor Controller, Interleaved*, Rev. 1 — June 2025, [www.onsemi.com/download/data-sheet/pdf/ncp1632a--d.pdf]
17. NXP, *TEA2017AAT/3 Digital configurable LLC and multimode PFC controller*, Rev. 1.2 — 30 August 2023. [www.nxp.com/docs/en/data-sheet/TEA2017AAT_3.pdf].
18. ON Semiconductor, *NCP1618 High-Voltage, Multimode, Power Factor Controller*, Rev. 9 — April 2025, [www.onsemi.com/download/data-sheet/pdf/ncp1618-d.pdf].
19. STMicroelectronics, *L6562AT Transition-mode PFC controller*, Rev. 9 — March 2009. [www.st.com/resource/en/datasheet/l6562at.pdf].
20. ON Semiconductor, *NCP1680 Totem Pole CrM Power Factor Correction Controller*, Rev. 1 — July 2024, [www.onsemi.com/download/data-sheet/pdf/ncp1680-d.pdf].
21. ON Semiconductor, *NCP1681 Totem Pole Multi−Mode Power Factor Correction Controller*, Rev. 1 — May 2023, [www.onsemi.com/download/data-sheet/pdf/ncp1681-d.pdf].
22. ON Semiconductor, *NCP1681CCM1KWGEVB Evaluation Board*, [www.onsemi.com/design/evaluation-board/NCP1681CCM1KWGEVB].

Analiza popularnych topologii korekcji współczynnika mocy w zasilaczach impulsowych

Streszczenie: Nieliniowe charakterystyki obciążenia, typowe dla przetwornic impulsowych, przekładają się na podwyższony poziom zniekształceń harmonicznych w sieci prądu przemiennego. Wynikające z tego pogorszenie jakości energii musi być korygowane przez zastosowanie korekcji współczynnika mocy PFC (ang. Power Factor Correction), często implementowanej w postaci dodatkowych modułowych układów elektronicznych. Najpowszechniej stosowanym rozwiązaniem są aktywne obwody PFC, składające się z elementów indukcyjnych i tranzystorów mocy, które regulują oraz kształtują prąd wejściowy przetwornicy tak, aby odpowiadał zarówno kształtem, jak i fazą napięciu wejściowemu. Modelowanie kształtu prądu sieciowego może być realizowane za pomocą różnych topologii PFC, w połączeniu z różnymi trybami przewodzenia cewki PFC. Niniejsza praca przedstawia przegląd układów PFC, w tym topologii typu boost, konfiguracji opartej na topologii flyback oraz bezmostkowej architektury typu totem-pole, znanej z wysokiej sprawności przetwarzania energii. Zaprezentowano szczegółową analizę teoretyczną problemu korekcji współczynnika mocy oraz opis głównych cech operacyjnych badanych topologii PFC. Badania zostały dodatkowo zilustrowane zrzutami ekranu z oscyloskopu, wykonanymi dla rzeczywistych, fizycznych modułów PFC zaprojektowanych przez autora (topologie typu boost i flyback) lub pozyskanych na potrzeby niniejszego artykułu. Badania te stanowią część projektu finansowanego przez Narodowe Centrum Badań i Rozwoju w ramach programu LIDER XV, na podstawie umowy o wykonanie i finansowanie projektu nr LIDER15/0205/2024.

Słowa kluczowe: elektronika mocy, przetwornice AC/DC, korekcja współczynnika mocy, bezmostkowa topologia typu totem-pole, straty mocy

Rafał Kasikowski, PhD Eng.
rafal.kasikowski@p.lodz.pl
ORCID: 0000-0002-2815-1746

He received the M.Sc. degree in electrical engineering in 2002 from the Technical University of Czestochowa, Poland, and he has also earned the M.Sc. degree in energy engineering in 2013 from the University of East Anglia, Norwich, United Kingdom. In 2021 he received the PhD degree in electronics from Lodz University of Technology, Poland, where he is currently working as a postdoctoral researcher. His research interests include modelling and optimization of Switch Mode Power Supplies.